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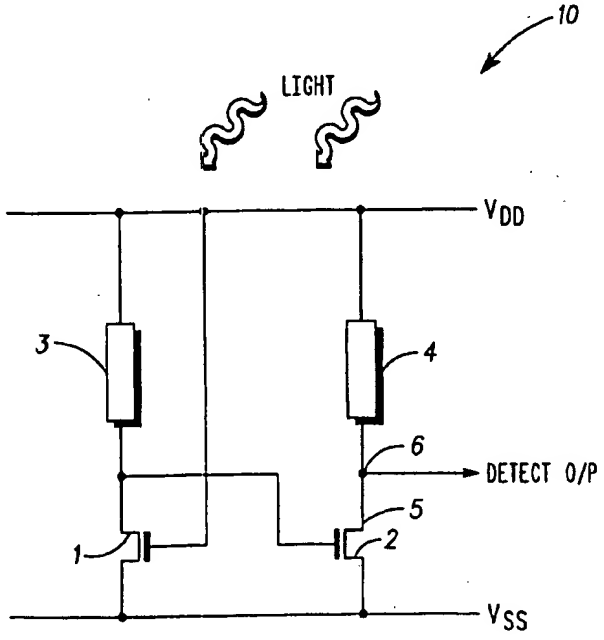
(54) Title: LIGHT DETECTION DEVICE

(57) Abstract

A light detection device has a biasing transistor (1) arranged to provide a bias current and a reverse biased transistor. The reverse biased transistor has a drain terminal (6) coupled via a high impedance resistor (4) to the supply voltage. Incident visible light is detected by a voltage drop at the drain electrode.



LIGHT DETECTION DEVICE

Field of the Invention

This invention relates to light detection devices and particularly but not exclusively to light detection devices for use in tamper detection applications.

Background of the Invention

In a semiconductor integrated circuit (IC), such as a banking smartcard, the IC is vulnerable to a breach of security if it falls into the hands of a dishonest person. The IC may be reverse engineered in order to reveal or modify functions and confidential data contained therein. It is known that such IC's have been decapsulated and have even undergone depassivation of the upper protective layer.

US patent 4,952,796 describes a circuit which comprises a current generator delivering current which flows into a reversed biased transistor junction. If subject to light, the reverse current in the junction increases, and the voltage at the junction terminals drops.

A problem with this arrangement is that incident light will generate reverse currents in transistors 11 and 2 of FIG.1, and this may affect the voltage drop detected at the output. Furthermore, the biasing and current generation functions of the above circuit are more susceptible to manufacturing process variations.

Also current drain, particularly in a smartcard, should be kept to a minimum, and the reverse current adversely affects the current consumption of the device. Lastly, the above circuit takes up much valuable semiconductor area, and again this is disadvantageous in a smartcard, where demand for space is at a premium.

This invention seeks to provide a light detection device which mitigates the above mentioned disadvantages.

Vdd via a second high impedance resistor 4, and further coupled to an output terminal 6. The high impedance resistor 4 is an undoped polysilicon resistor.

In operation, the gate terminal of the second transistor 2 is arranged to be reverse biased by receiving the bias current from the drain terminal of the first transistor 1.

When the drain terminal 5 of the second transistor is subjected to incident visible light, a small reverse current is generated between drain 5 and the ground terminal Vss. This current flow lowers the voltage at drain 5, and this voltage drop is detected by circuitry (not shown) coupled to the output terminal 6.

Since the second high impedance resistor is an undoped polysilicon resistor, extremely small currents can be detected, making the device 10 very sensitive to incident light.

No parasitic reverse currents are generated, and during the manufacturing process of the device 10, only one resistivity process is required to fabricate the first and the second high impedance resistors 3 and 4, and this will not introduce variations which will significantly affect the performance of the device 10.

It will be appreciated that alternative embodiments to the one described above are possible. For example, the biasing arrangement may vary from the precise configuration described above. In addition, the first and second resistors could be fabricated from a material other than undoped polysilicon.

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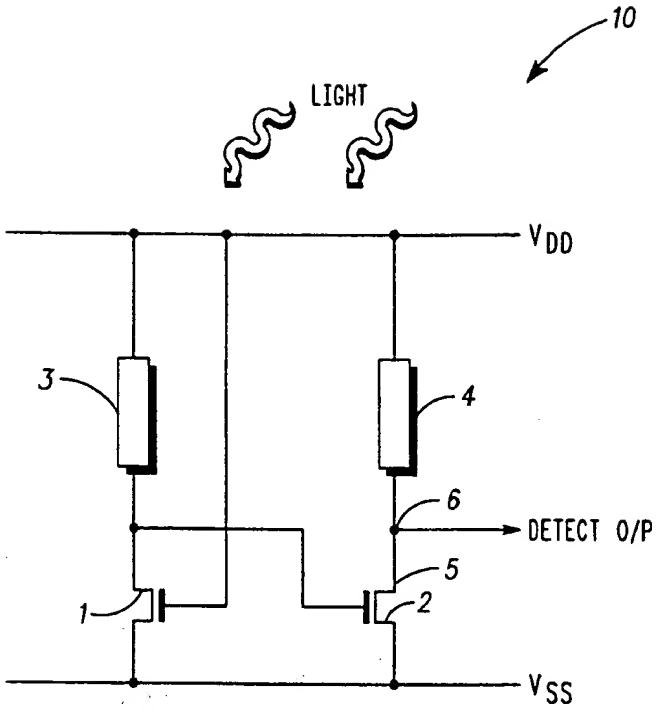

FIG.1